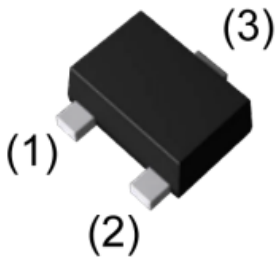
SSC8164GS9

N-Channel Small Switching MOSFET with ESD Protection

➢ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$ Typ.	I_D	ESD
60V	±20V	1Ω@10V	0.3A	500V
		1.25Ω@4V5		

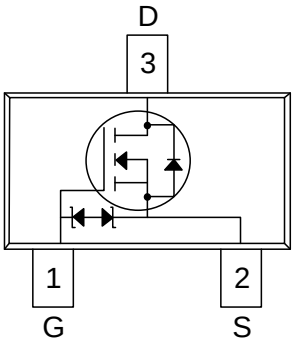
➢ Pin configuration



SOT-723

➢ Description

This device is an N-Channel enhancement mode MOSFET, with low on-resistance, fast switching speed and low threshold voltage, it is ideal for portable equipment.



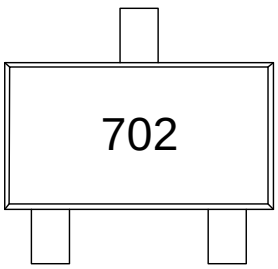
Pin Configuration (Top View)

➢ Applications

- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers
- Display, Memories, Transistors, etc.
- Battery Operated System
- Solid-State Relays

➢ Ordering Information

Device	Package	Shipping
SSC8164GS9	SOT-723	8000/Reel



Marking

➢ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	60	V
V_{GSS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current [a]	0.3	A
I_{DM}	Pulsed Drain Current [b]	0.8	A
P_D	Power Dissipation [c]	0.5	W
P_{DSM}	Power Dissipation [a]	0.25	W
T_J	Operation junction temperature	-55~150	℃
T_{STG}	Storage temperature range	-55~150	℃

➢ Thermal Resistance Ratings (T_A=25℃ unless otherwise noted)

Symbol	Parameter	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]	510	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	255	℃/W

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper, in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.

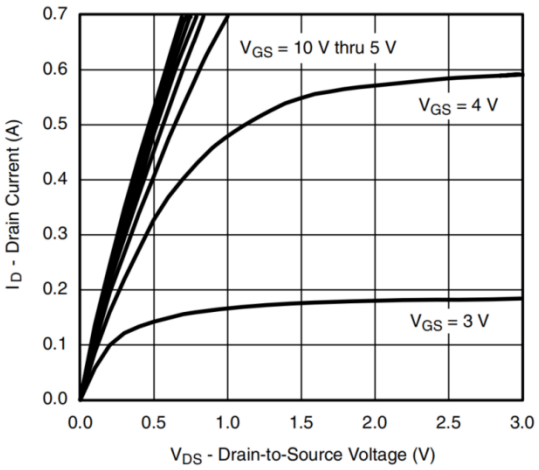
b. Repetitive rating, pulse width limited by junction temperature.

c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

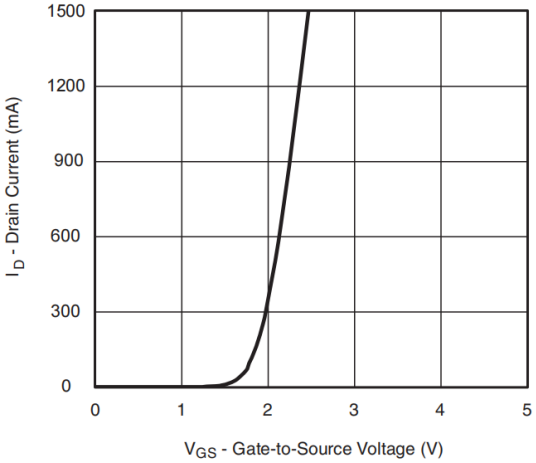
➢ Electrical Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	0.75	1	1.25	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 0.5A		1	2.5	Ω
		V_{GS} = 4.5V, I_D = 0.5A		1.25	3.5	
		V_{GS} = 2.5V, I_D = 0.2A		1.7	4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V			1	μA
Gate-Source Leak Current	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±10	μA
Transconductance	G_{FS}	V_{DS} = 10V, I_D = 0.2A		0.1		s
Forward Voltage	V_{SD}	V_{GS} = 0V, I_S = 0.2A			1.3	V
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		30		pF
Output Capacitance	C_{OSS}			6		
Reverse Transfer Capacitance	C_{RSS}			2.9		
Turn-on Delay Time	$T_{D(ON)}$	V_{GS} = 10V, V_{DS} = 10V, I_D = 0.1A		25		ns
Rise Time	T_r			10		
Turn-off Delay Time	$T_{D(OFF)}$			35		
Fall Time	T_f			20		
Total Gate Charge	Q_G	V_{GS} = 10V, V_{DS} = 15V, I_D = 0.2A		0.4		nC
Gate to Source Charge	Q_{GS}			0.1		
Gate to Drain Charge	Q_{GD}			0.11		

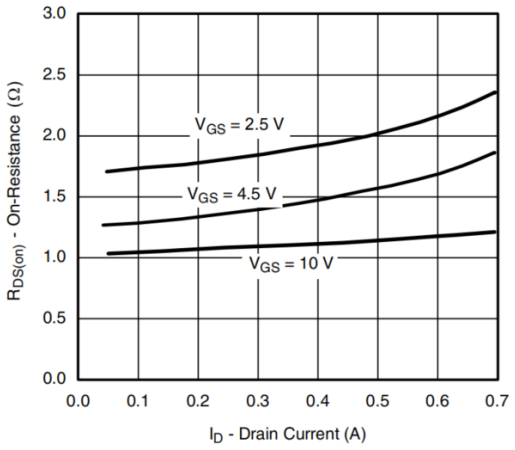
➢ Typical Performance Characteristics (T_A=25℃ unless otherwise noted)



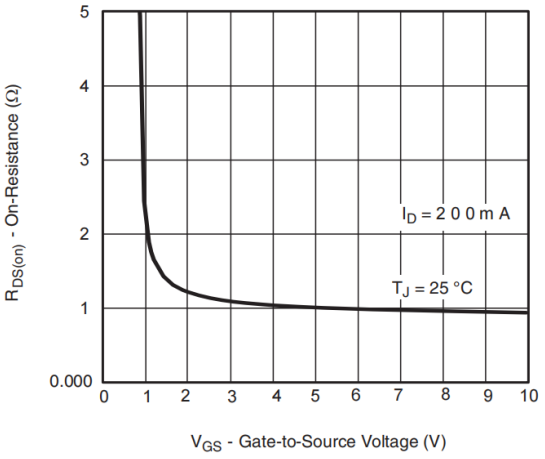
Output Characteristics



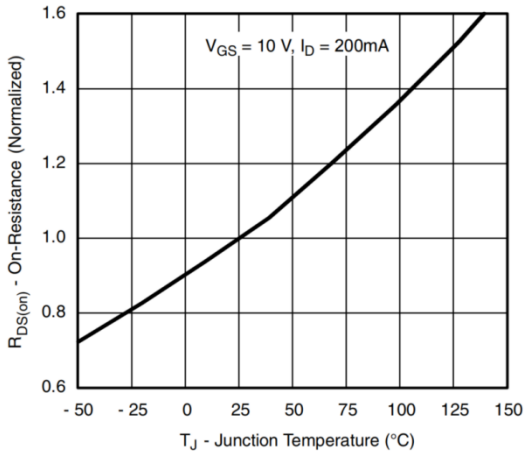
Transfer Characteristics



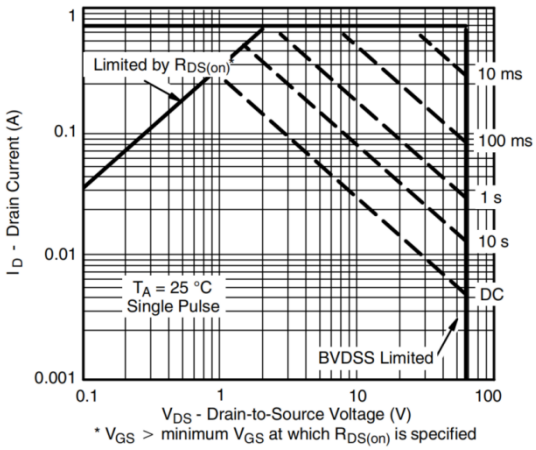
On-Resistance vs. Drain Current



On-Resistance vs. Gate-to-Source Voltage

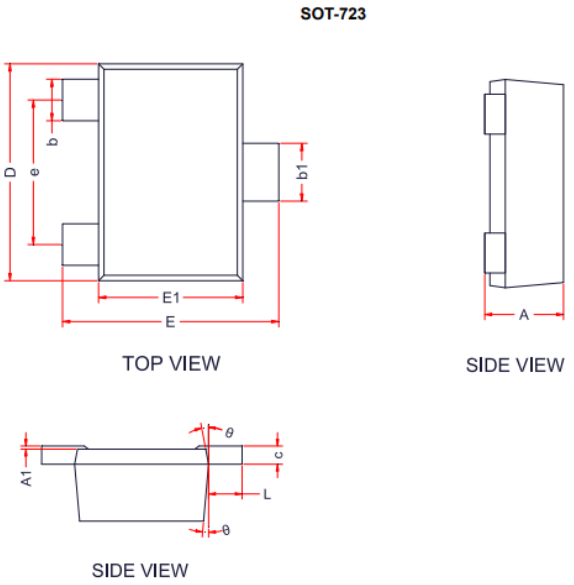


On-Resistance vs. Junction Temperature



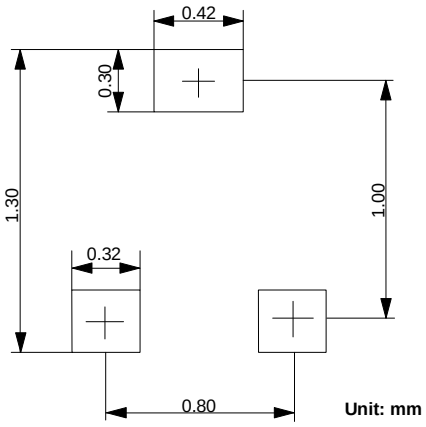
Safe Operating Area

➢ Package Information



DIM	Millimeters		
	Min.	Typ.	Max.
A	0.43	-	0.55
A1	0.00	-	0.05
b1	0.27		0.37
b	0.17	-	0.27
c	0.08	0.13	0.18
D	1.15	1.20	1.25
E	1.15	1.20	1.25
E1	0.75	0.8	0.85
e	0.80Ref.		
L	0.15	0.2	0.25
θ	7°Ref.		

➢ Suggested Pad Layout



➢ History Version

V2.0	First edition	2021-5-08
V2.1	Modify Typical Performance Characteristics	2023-12-22

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